CPE/CSC 142

Term Project

Phase 2

Tyler Moua: 33% Contribution

Aaron Rai: 33% Contribution

Micaela Varquez: 33% Contribution

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BCHazardControlUnit…………………………………….

ControlUnit…………………………………….

RegisterForwardingUnit…………………………………….

Verilog Source Code………………………………………..

ALUControlUnit…………………………………….

BCHazardControlUnit…………………………………….

BranchEquator…………………………………….

ControlUnit…………………………………….

CPU…………………………………….

DataMemory…………………………………….

EXMEM…………………………………….

IDEX…………………………………….

IFID…………………………………….

InstructionMemory…………………………………….

MainALU…………………………………….

MEMWB…………………………………….

MUX1-7…………………………………….

PC…………………………………….

RegisterFile…………………………………….

RegisterForwardingUnit…………………………………….

ShiftLeft…………………………………….

SignExtentions…………………………………….

ZeroExtend…………………………………….

Stimulus Module Used...…………………………………………………………………………

***CSc/CPE 142***

***Term Project Status Report***

***Team #13***

Complete this form by typing the requested information and include the completed form in your report after TOC. Gray cells will be filled by the instructor.

|  |  |  |
| --- | --- | --- |
| *Name* | *% Contribution* | *Grade* |
| *Tyler Moua* | *33* |  |
| *Aaron Rai* | *33* |  |
| *Micaela Varquez* | *33* |  |

***Please do not write in the first table***

|  |  |
| --- | --- |
| *Project Report/Presentation 20%* | /200 |
| *Functionality of the individual components 40%* | /400 |
| *Functionality of the overall design 25%* | /250 |
| *Design Approach 5%* | /50 |
| Total points | /900 |

**A: List all the instructions that were implemented correctly and verified by the assembly program on your system:**

| Instructions | Was this instruction fully fuctional as verified by the assembly program provided? If no, explain. This refres to validation using the complete CPU and not its components. |
| --- | --- |
| Signed addition | Yes |
| Signed subtraction | Yes |
| Move | Yes |
| SWAP | Yes |
| AND immediate | Yes |
| OR immediate | Yes |
| Load byte unsigned | Yes |
| Store byte | Yes |
| Load | Yes |
| Store | Yes |
| Branch on less than | Yes |
| Branch on greater than | Yes |
| Branch on equal | Yes |
| jump | Yes |
| halt | Yes |

**B: Fill out the next table:**

| Individual Components | Does your system have this component? | List the student who designed and verified the block | Does it work? | List problems with the component, if any. |
| --- | --- | --- | --- | --- |
| ALU | Yes | Tyler | Yes |  |
| ALU control unit | Yes | Tyler | Yes |  |
| Memory Unit | Yes | Aaron | Yes |  |
| Register File | Yes | Aaron | Yes |  |
| PC | Yes | Micaela | Yes |  |
| IR | Yes | Micaela | Yes |  |
| Other registers | No |  |  |  |
| Multiplexors | Yes | Micaela | Yes |  |
| exception handler  1. Unknown opcode  2. Arith. Overflow  ….. | Yes | Tyler  Aaron  Micaela | Yes |  |
| Control Units   1. main 2. forwarding 3. lw hazard detection | Yes | Tyler  Aaron  Micaela | Yes | Flush occurs 1 stage later than expected |

How many stages do you have in your pipeline? 5

C: **State any issue regarding the overall operation of the datapath? Be Specific.**

**With a flush, the subsequent instruction must first enter the ID stage of the pipeline before the pipeline is flushed. The Result of operation is correct, however.**